ABLUE TECHNOLOGY

PTR9814PA

Bluetooth 5 ready multi-protocol Module with PA Dual-Antenna, Embedded Cortex™ M4F 32 bit processor Support Bluetooth Direct Finding AOA/AOD, Support Zigbee,Thread,MESH,Matter,ANT Ideal choice of IoT and Smart product

The PTR9814PA ultra-low power Bluetooth 5 ready multiprotocol System on Module , designed for longer distance communication, built-in maximum + 20dBm RF output, based on the nRF52833 from Nordic Semiconductor. The module can support Bluetooth 5.2 by upgrading the protocol stack. The module with an ARM® Cortex™ M4F 32 bit processor, Bluetooth 5.1 Direct Finding AOA/AOD support， embedded 2.4GHz transceiver, provide a complete solution with no additional RF design, Bluetooth 5, ANT/ANT+, Matter, 802.15.4 and 2.4GHz proprietary multiprotocol support, allowing faster time to market, while simplifying designs, reducing BOM costs, also reduce the burden of Regulatory approvals to enter the world market. Making you more quickly into the Bluetooth smart application and remove the worries.

Features

- Nordic nRF52833 with ARM Cortex M4F
- nRF21540 RF front-end with PA and LNA
- Multiprotocol support : Bluetooth5, ANT/ANT+, and 2.4GHz proprietary, 802.15.4 Thread, Matter and Zigbee
- Bluetooth 5.1 Direction Finding AOA/AOD
- Bluetooth 5: 2 /1Mbps, 500 kbps, 125 kbps
- IEEE 802.15.4-2006: 250 kbps
- Proprietary 2.4 GHz: 2 Mbps, 1 Mbps
- Integrated DC-DC converter
- Serial Wire Debug (SWD)
- Nordic SoftDevice Ready
- Over-the-Air (OTA) firmware update
- Flash/RAM: 512KB/128KB.
- 40 General purpose I/O pins(reserve 9 I/O for RF front-end control)
- 15 level low-power comparator with wake-up from System OFF mode
- Two 2-wire Master/Slave (I2C compatible)
- I2S audio interface
- 12 bit/200KSPS ADC
- High-speed 32 MHz SPI
- 4 SPI Master/ 3 SPI Slave)
- 2 UART (with CTS/RTS and DMA)
- 4x 4-channel PWM unit with EasyDMA
- USB 2.0 full speed (12 Mbps) controller
- 20 channel CPU independent Programmable Peripheral Interconnect (PPI).
- Quadrature Demodulator (QDEC)
- 128-bit AES HW encryption
- 5 x 32 bits timers, 3 xReal Time Counters (RTC)
- NFC-A tag interface for OOB pairing
- Sizes:24.3x17.5 x2.5mm（include chip antenna）
- DC/DC on board
- No external components required
- Operation voltage: 2.7V to 3.6V
- Dual Antenna interface: one IPX Antenna, one on-board chip Antenna

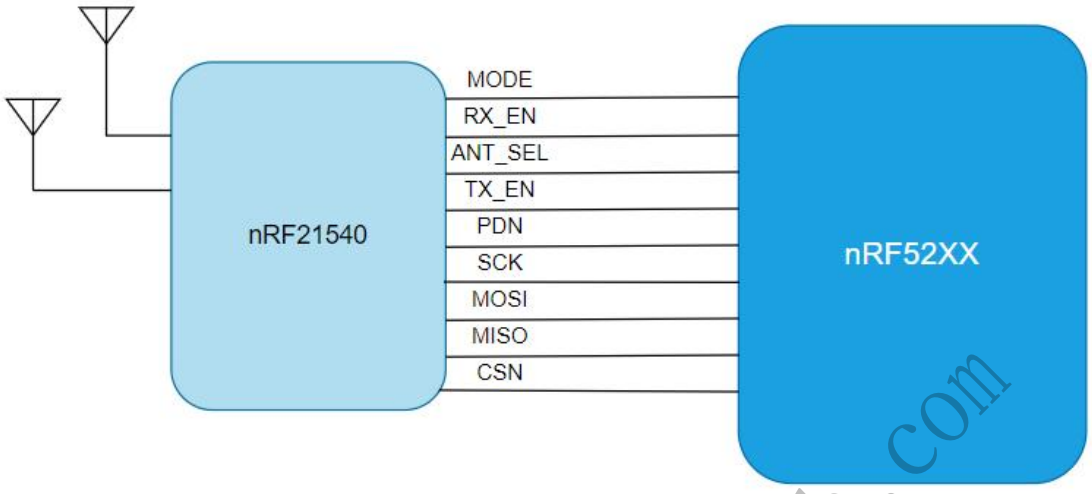
Typical Applications:

- 2.4 GHz Bluetooth low energy systems
- 2.4 GHz Proprietary systems
- Sports and leisure equipment
- Mobile phone accessories, Connected Appliances
- Health Care and Medical
- Consumer Electronics, Game pads
- Human Interface Devices, Remote control
- Building environment control / monitoring
- RFID, Security Applications，Low-Power Sensors
- Bluetooth Low Energy GateWay
- iBeacons™, Indoor navigation
- Lighting Products
- Fitness devices, Wearables

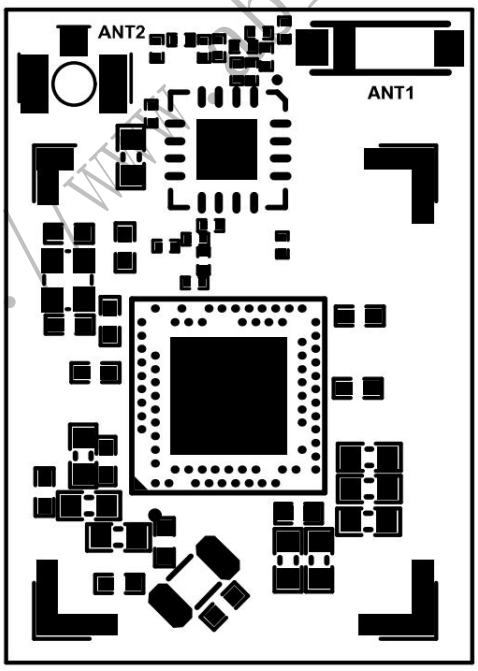
Quick Specifications:

Multi-protocol	
Version	Bluetooth 5 and Higher
Security	AES-128
Radio	
Frequency	2.360GHz to 2.500GHz
Modulations	GFSK at 2/1 Mbps, Long range 125/500kbps, 802.15.4- 250 kbps
Transmit power	Max +20dBm @setting nRF52833 0dBm output
Receiver sensitivity	-103dBm@BLE 125kbps(long range), -96dBm@BLE 1M
Antenna	Ext. IPX Antenna and On-board Chip Antenna
Current Consumption	
TX only @ +20 dBm	~100 mA
RX only @ 1 Mbps @ 3V, DC/DC enabled	~7.5mA（RF front-end enable）
CPU @ 64MHz from flash @ 3V, DC/DC	3.3 mA
System On	1.5 μA
System Off	0.6μA
Operating conditions	
Power supply	2.7~3.6V
Operating temperature	-25~+85 °C

Block diagram:



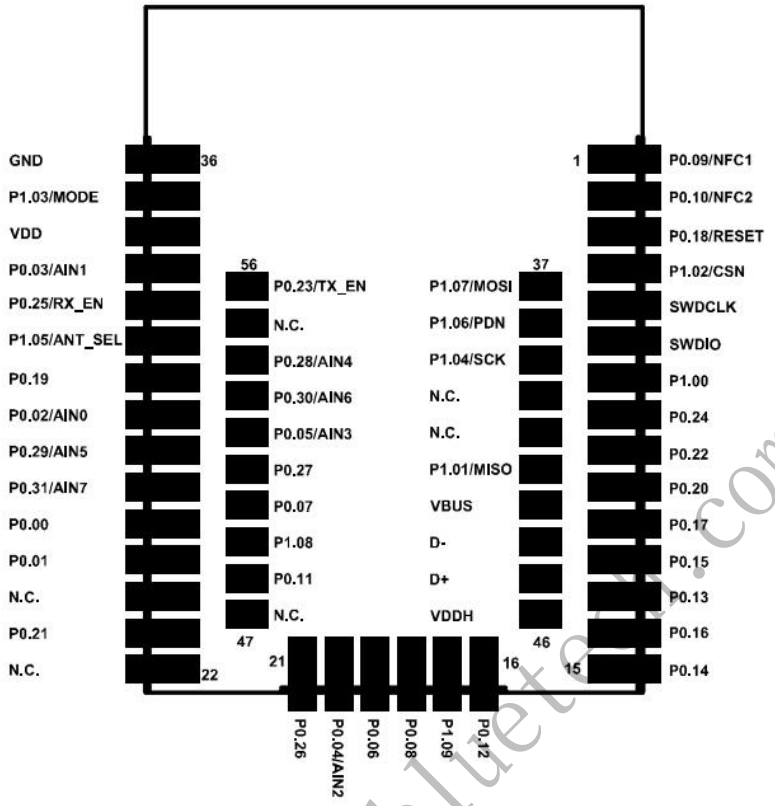
Module Top View:



ANT1: On board Chip Antenna.

ANT2: External IPX Antenna.

Pin Description of Module（Top View）:



Pin	Name	Description	Recommend usage
Pin1	P0.09/NFC1	Digital I/O/ NFC input	Standard drive, low frequency I/O
Pin2	P0.10/NFC2	Digital I/O/ NFC input	Standard drive, low frequency I/O
Pin3	P0.18/RESET	Digital I/O/RESET	
Pin4	P1.02	Digital I/O	Standard drive, low frequency I/O, Reserved for control PA/LNA internal
Pin5	SWDCLK	HW debug and programming	
Pin6	SWDIO	HW debug and programming	
Pin7	P1.00	Digital I/O	
Pin8	P0.24	Digital I/O	
Pin9	P0.22	Digital I/O	
Pin10	P0.20	Digital I/O	
Pin11	P0.17	Digital I/O	
Pin12	P0.15	Digital I/O	
Pin13	P0.13	Digital I/O	
Pin14	P0.16	Digital I/O	
Pin15	P0.14	Digital I/O	
Pin16	P0.12	Digital I/O	
Pin17	P1.09	Digital I/O	
Pin18	P0.08	Digital I/O	
Pin19	P0.06	Digital I/O	
Pin20	P0.04/AIN2	Digital I/O/Analog input 2	

Pin21	P0.26	Digital I/O	
Pin22	NC	NC	
Pin23	P0.21	Digital I/O	
Pin24	NC	NC	
Pin25	P0.01/XL2	Reserve for 32.768KHz use	
Pin26	P0.00/XL1	Reserve for 32.768KHz use	
Pin27	P0.31/AIN7	Digital I/O/Analog input 7	Standard drive, low frequency I/O
Pin28	P0.29/AIN5	Digital I/O/Analog input 5	Standard drive, low frequency I/O
Pin29	P0.02/AIN0	Digital I/O/Analog input 0	Standard drive, low frequency I/O
Pin30	P0.19	Digital I/O	Standard drive, low frequency I/O
Pin31	P1.05	Digital I/O	Standard drive, low frequency I/O, Reserved for control PA/LNA internal
Pin32	P0.25	Digital I/O	Standard drive, low frequency I/O, Reserved for control PA/LNA internal
Pin33	P0.03/AIN1	Digital I/O/Analog input 1	Standard drive, low frequency I/O
Pin34	VDD	Power Supply	
Pin35	P1.03	Digital I/O	Standard drive, low frequency I/O, Reserved for control PA/LNA internal
Pin36	GND	Ground	
Pin37	P1.07	Digital I/O	Standard drive, low frequency I/O, Reserved for control PA/LNA internal
Pin38	P1.06	Digital I/O	Standard drive, low frequency I/O, Reserved for control PA/LNA internal
Pin39	P1.04	Digital I/O	Standard drive, low frequency I/O, Reserved for control PA/LNA internal
Pin40	NC	NC	
Pin41	NC	NC	
Pin42	P1.01	Digital I/O	Standard drive, low frequency I/O, Reserved for control PA/LNA internal
Pin43	VBUS	Power	5 V input for USB 3.3 V regulator
Pin44	D-	USB D-	USB
Pin45	D+	USB D+	USB
Pin46	VDDH	High voltage power supply	
Pin47	NC	NC	
Pin48	P0.11	Digital I/O	
Pin49	P1.08	Digital I/O	
Pin50	P0.07	Digital I/O	
Pin51	P0.27	Digital I/O	
Pin52	P0.05/AIN3	Digital I/O/Analog input 3	
Pin53	P0.30/AIN6	Digital I/O/Analog input 6	Standard drive, low frequency I/O
Pin54	P0.28/AIN4	Digital I/O/Analog input 4	Standard drive, low frequency I/O
Pin55	NC	NC	
Pin56	P0.23	Digital I/O	Standard drive, low frequency I/O, Reserved for control PA/LNA internal

*Low frequency I/O is signals with a frequency up to 10 kHz
*The module needs to reserve 9 I/O of nRF52833 for nRF21540 RF front-end control， already internally connected on module，Please do not use these reserved pins for other purposes.

Note: An internal 4.7μF bulk capacitor has been included on the module. For those application that with heavy GPIO usage and/or current draw, it is good design practice to add additional bulk capacitance as required for your application.

General Purpose I/O:

Each GPIO can be accessed individually with the following user configurable features:

- Input/output direction
- Output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high or low level triggers on all pins
- Trigger interrupt on all pins
- All pins can be used by the PPI task/event system; the maximum number of pins that can be interfaced through the PPI at the same time is limited by the number of GPIOTE channels
- All pins can be individually configured to carry serial interface or quadrature demodulator signals

Hardware RESET:

There is on-chip power-on reset circuitry, But can still be used in external reset mode, in this case, GPIO pin P0.18 as an external hardware reset pin. In order to utilize P0.18 as a hardware reset, the UICR registers PSELRESET[0] and PSELRESET[1] must be set alike, to the value of 0x7FFFFF12. When P0.18 is programmed as RESET, the internal pull-up is automatically enabled.

HW debug and flash programming of Module :

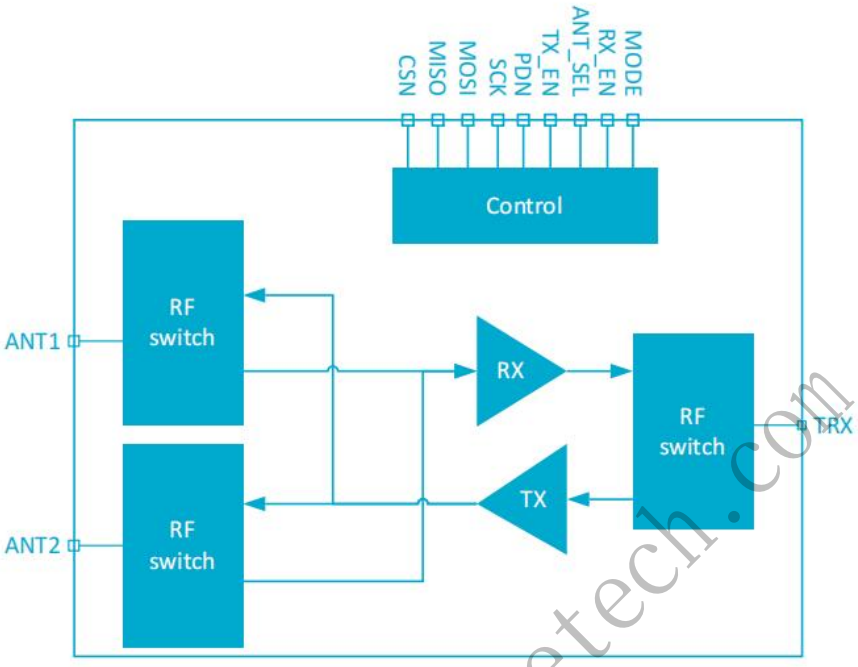
The Module support the two pin Serial Wire Debug (SWD) interface and offers flexible and powerful mechanism for non-intrusive debugging of program code. Breakpoints, single stepping, and instruction trace capture of code execution flow are part of this support.

Pin	Flash Program interface
SWDIO	Debug and flash programming I/O
SWDCLK	Debug and flash programming I/O

This is the hardware debug and flash programming of module, J-Link Lite support, please refer www.segger.com.

RF Front-end Hardware Connect and Software Control:

1. nRF21540 Block diagram



2. Hardware connection between nRF52833 and nRF21540

The nRF52833 needs to reserve 9 I/O for nRF21540 RF front-end control， already internally connected on module，Please do not use these reserved pins on nRF52833 for other purposes.

nRF52833	nRF21540
P1.03	MODE
P1.05	ANT_SEL
P0.25	RX_EN
P0.23	TX_EN
P1.06	PDN
P1.04	SCK
P1.07	MOSI
P1.01	MISO
P1.02	CSN

3. RF Front-end Control

nRF21540 uses an internal state machine to control the operation of the device. The state machine is controlled through GPIO control mode or through the SPI/GPIO control mode.

GPIO mode is that using the I/O to control nRF21540's state, this control mode is simple to use and use less I/O.

Through SPI control mode may need more I/O to control but can completely control and set all the parameters of nRF21540（eg. adjustable TX output gain）.

3.1 GPIO Mode

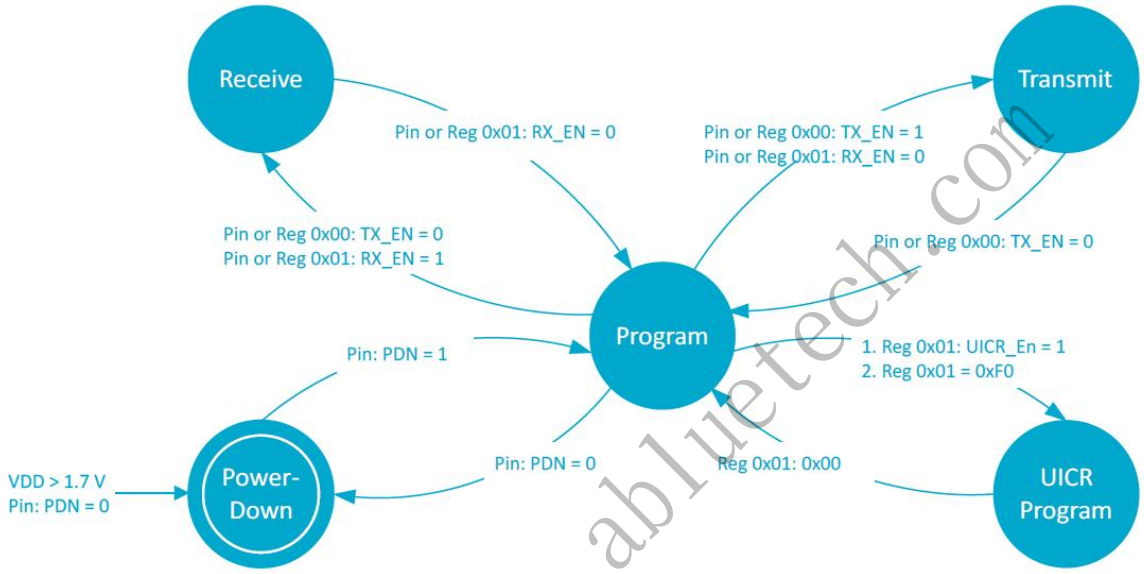
When PDN is set to 0, the device is in Power-down state. When PDN is set to 1, the device is activated and

enters Program state. All registers contain reset values when the device enters Program state. The device can be set to another state (Receive, Transmit, and UICR Program) using pin control or the SPI interface.

State transitions are controlled by pins PDN, RX_EN, and TX_EN.

When the device is in Receive state, the receive path is active and the transmit path is disabled. In the Receive state, the LNA is enabled.

When the device is in Transmit state, the transmit path is enabled and the receive path is disabled. In Transmit state, the PA is enabled.



State	Symbol	Description
Power-down	PD	The device is in Power-down state.
Program	PG	The device can be configured and set to other states.
UICR program	UICR	User defined initialization values for POUTA_SEL, POUTA_UICR, POUTB_SEL, and POUTB_UICR can be configured to UICR.
Receive	RX	The RX path is enabled.
Transmit	TX	The TX path is enabled.

3.2 SPI Mode

State transitions are controlled by bit fields in SPI registers CONFREG0 and CONFREG1.

UICR Program state enables programming to UICR EFUSE (one time programmable memory) of default settings for TX power control. UICR Program state is accessed from Program state by writing specific values to register CONFREG1. Registers CONFREG2 and CONFREG3 are for bit programming definition and triggering UICR EFUSE programming.

Register	Function	Accessible via SPI in the following states
CONFREG0	TX state control and TX gain control in Program state	PG, RX, TX, UICR
CONFREG1	RX state control in Program state	PG, RX, TX, UICR
CONFREG2, CONFREG3	UICR programming interface registers	UICR
PARTNUMBER, HW_REVISION[7:4]	Part number, hardware revision	PG
HW_ID0, HW_ID1	Hardware ID	PG

3.3 Antenna Selects Control

ANT_SEL selects the antenna interface used during RX or TX. Antenna interface control is specified in the following table.

In this module, ANT1: On board Chip Antenna. ANT2: External IPX Antenna.

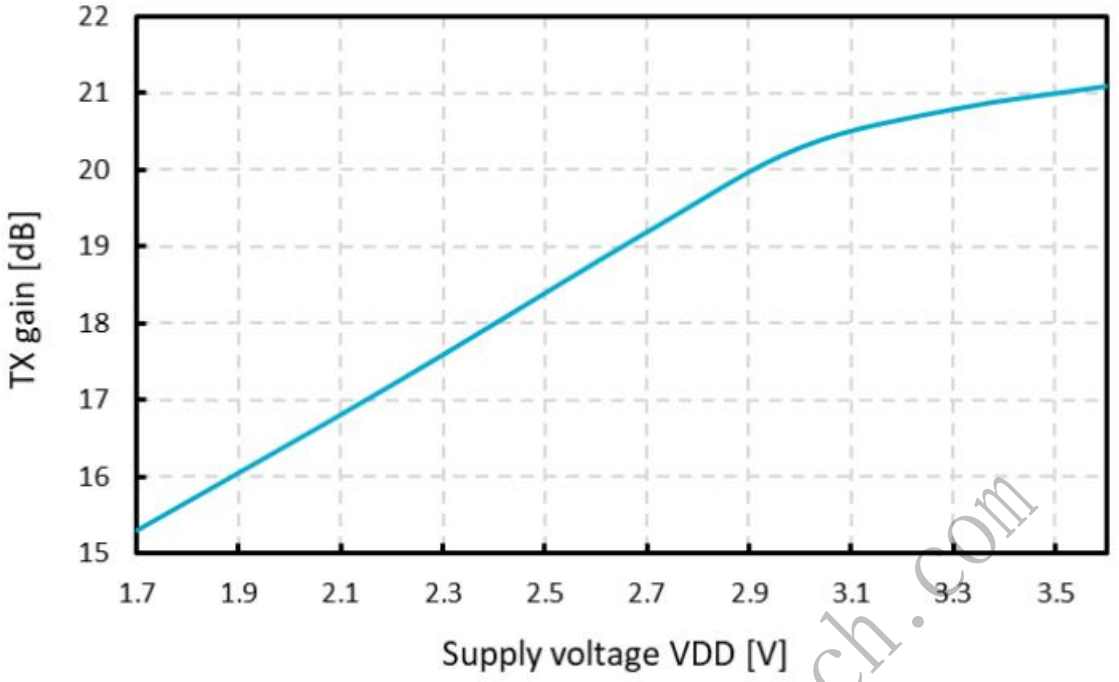
State	ANT_SEL	Description
Power-down	X	Antenna switches disabled (isolating)
Program	X	Antenna switches disabled (isolating)
UICR program	X	Antenna switches disabled (isolating)
Receive	0	ANT1 enabled, ANT2 disabled
	1	ANT1 disabled, ANT2 enabled
Transmit	0	ANT1 enabled, ANT2 disabled
	1	ANT1 disabled, ANT2 enabled

3.4 TX Gain

Custom preset values are stored in UICR and selected as default by writing to the MODE bit in CONFREG0 use SPI control.

The following figure shows the TX gain over VDD, with register ONFREG0.TX_GAIN=POUTA_PROD (20 dB).

The working voltage of nRF21540 is recommended to use 2.7~3.6v. It can support 1.7~3.6v, the output power will be reduced.



3.5 Current Consumption

Symbol	Description	Min.	Typ.	Max.	Units
I_{PD}	State: PD		45		nA
I_{PG}	State: PG		1.1		mA
I_{RX}	State: RX		2.9		mA
I_{TX_10dBm}	State: TX P_{OUT} = 10 dBm		38		mA
I_{TX_20dBm}	State: TX P_{OUT} = 20 dBm		110		mA

4. The RF Front-end control samples code with NCS 2.0

FEMs provide a power amplifier (PA) that increases the TX power and a low-noise amplifier (LNA) that increases the RX sensitivity. Some FEMs, like the nRF21540, also provide a power down (PDN) control that powers down the FEM internal circuits, to reduce energy consumption.

This guide describes how to add support for 2 different front-end module (FEM) implementations to your application in nRF Connect SDK. To use radio protocols and a FEM with your application, enable Front-end module feature in the Multiprotocol Service Layer (MPSL) library.

4.1 Using MPSL

The library provides multi-protocol support, but you can also use it in applications that require only one protocol. To avoid conflicts, check the protocol documentation to see if the protocol uses the FEM support provided by MPSL.

4.1.1 Enabling FEM and MPSL

Before you add the devicetree node in your application, complete the following steps:

- Add support for the MPSL library in your application. The MPSL library provides API to configure FEM. See Integration notes in the nrfxlib documentation for details.
- Enable support for MPSL implementation in nRF Connect SDK by setting the CONFIG_MPSL Kconfig option to y.
- Enable support for the FEM subsystem in nRF Connect SDK by setting the CONFIG_MPSL_FEM Kconfig option to y.
- Choose the used FEM implementation by selecting the appropriate Kconfig option.

The following FEM implementations are supported:

- The nRF21540 GPIO implementation, see GPIO mode. To use it, set the CONFIG_MPSL_FEM_NRF21540_GPIO Kconfig option to y.
- The nRF21540 GPIO SPI implementation, see SPI/GPIO mode. To use it, set the CONFIG_MPSL_FEM_NRF21540_GPIO_SPI Kconfig option to y.
- The nRF21540 2-pin simple GPIO implementation. To use it, set the CONFIG_MPSL_FEM_SIMPLE_GPIO Kconfig option to y.

4.1.2 Setting the FEM output power

The tx_gain_db property in devicetree provides the FEM gain value to use with the simple GPIO FEM implementation. The property must represent the real gain of the FEM. This implementation does not support controlling the gain value during runtime.

nRF21540 implementations have the gain set to 10 by default. You can set a different gain value to use through the CONFIG_MPSL_FEM_NRF21540_TX_GAIN_DB option, but it has to match the value of one of the POUTA (CONFIG_MPSL_FEM_NRF21540_TX_GAIN_DB_POUTA) or POUTB (CONFIG_MPSL_FEM_NRF21540_TX_GAIN_DB_POUTB) gains.

CONFIG_MPSL_FEM_NRF21540_TX_GAIN_DB_POUTA and CONFIG_MPSL_FEM_NRF21540_TX_GAIN_DB_POUTB are by default set to 20 and 10 and these are factory-precalibrated gain values. Do not change these values, unless POUTA and POUTB were calibrated to different values on specific request.

To enable runtime control of the gain, set the CONFIG_MPSL_FEM_NRF21540_RUNTIME_PA_GAIN_CONTROL to y.
This option makes the gain of the FEM to be adjusted dynamically during runtime, depending on the power requested by the protocol driver for each transmission. For the nRF21540 GPIO implementation, you must enable the MODE pin in devicetree. For the nRF21540 GPIO SPI implementation, no additional configuration is needed as the gain setting is transmitted over the SPI bus to the nRF21540.

You can use only the Front-end module feature API if your application does not require other MPSL features. This might be useful when you want to run simple radio protocols that are not intended to be used concurrently with other protocols. Enable the following Kconfig options:

- CONFIG_MPSL
- CONFIG_MPSL_FEM_ONLY

4.1.3 Using FEM power models

When a protocol driver requests a given transmission power to be output, MPSL splits the power into the following components: the SoC Power and the FEM gain. This gain is considered constant and accurate even if external conditions, such as temperature, might affect the effective gain achieved by the Front-End Module.

To perform the split differently (for example, to compensate for external conditions), you can use a FEM power model, either using one of the built-in ones or providing your own custom model.

To use FEM power models, set the CONFIG_MPSL_FEM_POWER_MODEL Kconfig option to y and either select one of the built-in models or provide a custom model, as described in the following chapters.

4.1.4 Using nRF21540 GPIO SPI built-in power model

To use this model, set CONFIG_MPSL_FEM_POWER_MODEL and CONFIG_MPSL_FEM_POWER_MODEL_NRF21540_USE_BUILTIN to y.

This feature uses a model to compensate the FEM gain for the following external conditions:

- Temperature
- FEM supply voltage
- Carrier frequency
- FEM input power.

The model assumes that the FEM supply voltage is constant. To provide the value of this voltage to the MPSL subsystem, use the CONFIG_MPSL_FEM_POWER_VOLTAGE option.

4.1.5 Adding custom power models

If the way MPSL splits the TX power into components does not meet your requirements, or if you wish to implement a custom compensation model, you can provide one as follows:

- Set CONFIG_MPSL_FEM_POWER_MODEL to y
- Provide an implementation of the mpsl_fem_power_model_to_use_get() function. This function should return a pointer to a variable of the type mpsl_fem_power_model_t which contains pointers to the model's callbacks.
- Mandatorily implement the model's fetch callback (details explained below).
- Optionally implement the model's init callback (details explained below). If no init callback is provided, pass NULL as the pointer to the callback.
- You can also optionally extend the MPSL_FEM_POWER_MODEL_CHOICE Kconfig choice with an option to select your custom model, for example, if you want to test multiple custom models.

The init callback is called by MPSL once, after FEM configuration finishes. Calibration data (acquired from FEM internal registers, Kconfig options, and devicetree files) is passed to this function using a parameter of the mpsl_fem_calibration_data_t type. The meaning of the calibration data stored in this parameter is implementation-specific. For details, see the mpsl_fem_calibration_data_t type documentation.

The fetch callback is used to split the power between the SoC output power and the FEM gain. It is called every time this split needs to be recalculated. For 802.15.4, this happens before every transmission. For Bluetooth Low Energy, this happens every time the channel changes.

NOTE:
This function is called in a time-critical path. Please refer to the documentation of mpsl_fem_power_model_t on timing constraints. Any complex calculations have to be done outside this function (for example, using a look up table). Failing to meet the timing requirements will lead to an undefined behavior of the protocol stacks.

The fetch callback must fill out all the fields of the the p_output output parameter. For more details, see the mpsl_fem_power_model_output_t type documentation.

NOTE:
The soc_power field value must be one of the output power values supported by the given nRF SoC, otherwise the behavior is undefined. The user can meet this requirement by converting the requested SoC power using the mpsl_tx_power_radio_supported_power_adjust function.

4.2 Hardware description

The nRF Connect SDK provides a wrapper that configures FEM based on devicetree (DTS) and Kconfig information. To enable FEM support, you must add an nrf_radio_fem node in the devicetree file. The node can also be provided by the devicetree file of the target development kit or by an overlay file. See Devicetree for more information about the DTS data structure, and Devicetree versus Kconfig for information about differences between DTS and Kconfig.

4.2.1 GPIO mode

The nRF21540 GPIO mode implementation of FEM is compatible with this device and implements the 3-pin PA/LNA interface.

NOTE:
In the naming convention used in the API of the MPSL library, the functionalities designated as PA and LNA apply to the tx-en-gpios and rx-en-gpios pins listed below, respectively.

To use nRF21540 in GPIO mode, complete the following steps:

1. Add the following node in the devicetree file:

```
/ {
      nrf_radio_fem: name_of_fem_node {
         compatible  = "nordic,nrf21540-fem";
         tx-en-gpios = <&gpio0 13 GPIO_ACTIVE_HIGH>;
         rx-en-gpios = <&gpio0 14 GPIO_ACTIVE_HIGH>;
         pdn-gpios   = <&gpio0 15 GPIO_ACTIVE_HIGH>;
   };
};
```

2. Optionally replace the node name name_of_fem_node.

3. Replace the pin numbers provided for each of the required properties:

- tx-en-gpios - GPIO characteristic of the device that controls the TX_EN signal of nRF21540.
- rx-en-gpios - GPIO characteristic of the device that controls the RX_EN signal of nRF21540.
- pdn-gpios - GPIO characteristic of the device that controls the PDN signal of nRF21540.

These properties correspond to TX_EN, RX_EN, and PDN pins of nRF21540 that are supported by software FEM.

Type phandle-array is used here, which is common in Zephyr's devicetree to describe GPIO signals. The first element &gpio0 refers to the GPIO port ("port 0" has been selected in the example shown). The second element is the pin number on that port. The last element must be GPIO_ACTIVE_HIGH for nRF21540, but for a different FEM module you can use GPIO_ACTIVE_LOW.
The state of the remaining control pins should be set in other ways and according to nRF21540 Product Specification.

4. On nRF53 devices, you must also apply the same devicetree node mentioned in step 1 to the network core. To do so, apply the overlay to the correct network core child image by creating an overlay file named child_image/*childImageName*.overlay in your application directory, for example child_image/ multiprotocol_rpmsg.overlay.

The *childImageName* string must be one of the following values:

- multiprotocol_rpmsg for multiprotocol applications having support for both 802.15.4 and Bluetooth.
- 802154_rpmsg for applications having support for 802.15.4, but not for Bluetooth.
- hci_rpmsg for application having support for Bluetooth, but not for 802.15.4.

NOTE:
This step is not needed when testing with Bluetooth: Direct Test Mode and Radio test on the nRF53 Series devices.

4.2.2 SPI mode

The nRF21540 features an SPI interface. You can use it to fully control your front-end module or you can use a combination of SPI and GPIO interface. The SPI interface enables you, for example, to set the output power of the nRF21540.

To use nRF21540 in SPI or SPI/GPIO mixed mode, complete the following steps:
1. Add the following node in the devicetree file:

```
/ {
      nrf_radio_fem: name_of_fem_node {
         compatible  = "nordic,nrf21540-fem";
         tx-en-gpios = <&gpio0 13 GPIO_ACTIVE_HIGH>;
         rx-en-gpios = <&gpio0 14 GPIO_ACTIVE_HIGH>;
         pdn-gpios   = <&gpio0 15 GPIO_ACTIVE_HIGH>;
         spi-if = <&nrf_radio_fem_spi>
   };
};
```

2. Optionally replace the device name name_of_fem_node.

3. Replace the pin numbers provided for each of the required properties:

- tx-en-gpios - GPIO characteristic of the device that controls the TX_EN signal of nRF21540.
- rx-en-gpios - GPIO characteristic of the device that controls the RX_EN signal of nRF21540.
- pdn-gpios - GPIO characteristic of the device that controls the PDN signal of nRF21540.

These properties correspond to TX_EN, RX_EN, and PDN pins of nRF21540 that are supported by software FEM.

The``phandle-array`` type is commonly used for describing GPIO signals in Zephyr's devicetree. The first element &gpio0 refers to the GPIO port ("port 0" has been selected in the example shown). The second element is the pin number on that port. The last element must be GPIO_ACTIVE_HIGH for nRF21540, but for a different FEM module you can use GPIO_ACTIVE_LOW.

Set the state of the remaining control pins according to the nRF21540 Product Specification.

4. Add a following SPI bus device node on the devicetree file:

```
&pinctrl {
    spi3_default_alt: spi3_default_alt {
        group1 {
            psels = <NRF_PSEL(SPI_SCK, 1, 15)>,
                    <NRF_PSEL(SPI_MISO, 1, 14)>,
                    <NRF_PSEL(SPI_MOSI, 1, 13)>;
        };
    };

    spi3_sleep_alt: spi3_sleep_alt {
        group1 {
            psels = <NRF_PSEL(SPI_SCK, 1, 15)>,
                    <NRF_PSEL(SPI_MISO, 1, 14)>,
                    <NRF_PSEL(SPI_MOSI, 1, 13)>;
            low-power-enable;
        };
    };
};

fem_spi: &spi3 {
        status = "okay";
    pinctrl-0 = <&spi3_default_alt>;
    pinctrl-1 = <&spi3_sleep_alt>;
    pinctrl-names = "default", "sleep";
        cs-gpios = <&gpio0 21 GPIO_ACTIVE_LOW>;

        nrf_radio_fem_spi: nrf21540_fem_spi@0 {
                compatible = "nordic,nrf21540-fem-spi";
                status = "okay";
                reg = <0>;
                label = "FEM_SPI_IF";
                spi-max-frequency = <8000000>;
        };
};
```

In this example, the nRF21540 is controlled by the spi3 bus. Replace the SPI bus according to your hardware design.

5. Create alternative pinctrl entries for SPI3 and replace the pinctrl-N and pinctrl-names properties.

4.2.3 Optional properties

The following properties are optional and you can add them to the devicetree node if needed.

1. Properties that control the other pins:

- ant-sel-gpios - GPIO characteristic of the device that controls the ANT_SEL signal of the nRF21540.
- mode-gpios - GPIO characteristic of the device that controls the MODE signal of the nRF21540.

The MODE signal of the nRF21540 switches between two values of PA gain. The pin can either be set to a fixed state on initialization, which results in a constant PA gain, or it can be switched in run-time by the protocol drivers to match the transmission power requested by the application.

To enable run-time MODE pin switching, you must enable CONFIG_MPSL_FEM_NRF21540_ RUNTIME_PA_GAIN_CONTROL.

NOTE:
The state of the MODE pin is selected based on the available PA gains and the required transmission power. To achieve reliable performance, CONFIG_MPSL_FEM_NRF21540_TX_GAIN_ DB_POUTA and CONFIG_MPSL_FEM_NRF21540_TX_GAIN_DB_POUTB must reflect the content of the nRF21540 registers. Their default values match chip production defaults. For details, see the nRF21540 Product Specification.

If the run-time MODE pin switching is disabled, the PA gain is constant and equal to CONFIG_MPSL_FEM_NRF21540_TX_GAIN_DB.

2. Properties that control the timing of interface signals:

- tx-en-settle-time-us - Minimal time interval between asserting the TX_EN signal and starting the radio transmission, in microseconds.
- rx-en-settle-time-us - Minimal time interval between asserting the RX_EN signal and starting the radio transmission, in microseconds.

NOTE:
Values for these two properties cannot be higher than the Radio Ramp-Up time defined by TX_RAMP_UP_TIME and RX_RAMP_UP_TIME. If the value is too high, the radio driver will not work properly and will not control FEM. Moreover, setting a value that is lower than the default value can cause disturbances in the radio transmission, because FEM may be triggered too late.

- pdn-settle-time-us - Time interval before the PA or LNA activation reserved for the FEM ramp-up, in microseconds.
- trx-hold-time-us - Time interval for which the FEM is kept powered up after the event that triggers the PDN deactivation, in microseconds.

The default values of these properties are appropriate for default hardware and most use cases. You can override them if you need additional capacitors, for example when using custom hardware. In such cases, add the property name under the required properties in the devicetree node and set a new custom value.

NOTE:
These values have some constraints. For details, see nRF21540 Product Specification.

Power and Configuration:

The module has two internal regulator stages. REG1 regulator stage has the regulator type options of Low-dropout regulator (LDO) and Buck regulator (DC/DC). REG0 regulator stage has only the option of Low-dropout regulator (LDO). The first regulator, REG0, is fed by the VDDH pin and can accept a source voltage of 2.5 V to 5.5 V. The output of REG0 is connected to the VDD pin and the input of the second regulator stage REG1. REG1 supplies power to the module core and can accept an input source voltage of 1.7V to 3.6V. Depending on how the VDD and VDDH pins are connected, the module will operate in one of two modes: Normal/Low Voltage (LV) or High Voltage (HV). The voltage present on the VDD pin is always the GPIO high logic level voltage, regardless of power mode.

To enter LV Mode, the same source voltage is applied to both the VDD and VDDH pins causing REG0 to automatically shut down leaving only the REG1 stage active. To enter HV, the source voltage is only applied to VDDH causing the VDD pin to become an output source supplied by REG0.

Mode	Pin of Module	Name	Power Connection
Normal/Low Voltage (LV)	Pin 34	VDD	1.7V to 3.6V source in
	Pin 46	VDDH	Same source as VDD
High Voltage (HV)	Pin 34	VDD	1.8V to 3.3V supply out
	Pin 46	VDDH	2.5V to 5.5V source in

Important: In HV mode, the GPIO high voltage defaults to 1.8V (configurable by REGOUT0 register). In order to ensure that the voltage on the GPIO pins match each other when the module communicates with external devices, attention should be paid to the power supply of external devices: 1) The power supply voltage of the external equipment connected to the module should be consistent with the VDD of the module; 2) When the power supply voltage of the external equipment is not consistent with the VDD of the module, a conversion circuit should be used.

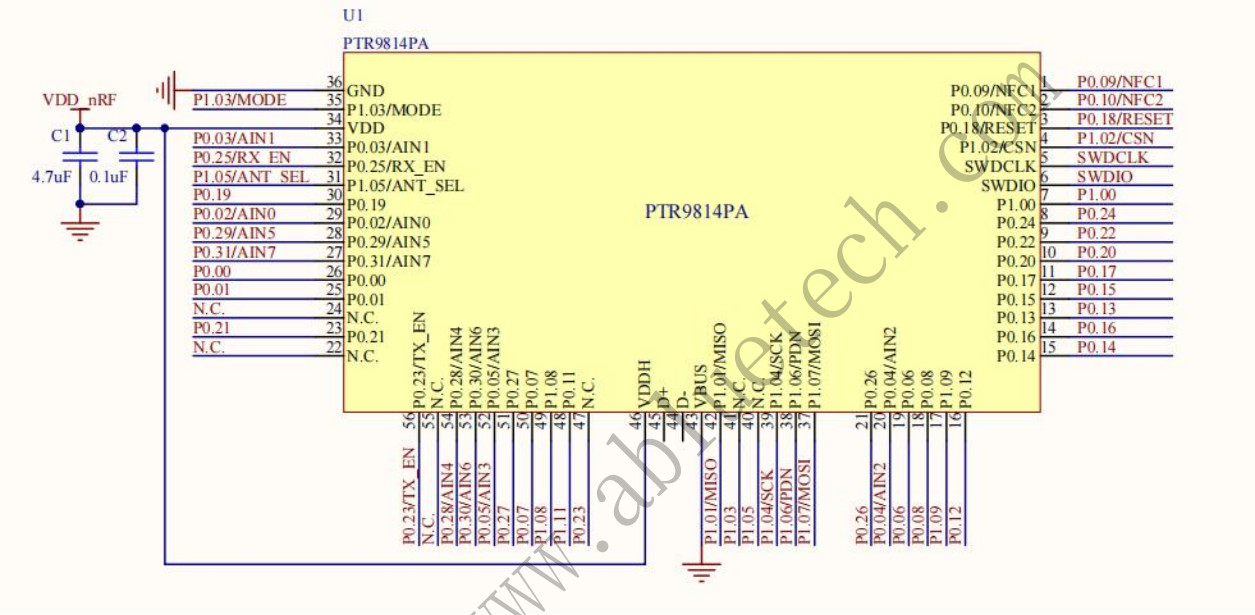
USB Power: The USB interface on the Module can be used when the module is in either Normal /Low Voltage (LV) or High Voltage (HV) mode. The Module USB PHY is powered by a dedicated, internal LDO regulator that is fed by the VBUS pin (Pin43). This means that applying power to only the VBUS pin will not power the rest of the module. In order for the USB PHY to operate, VBUS must be externally powered.

Reference circuitry:

In this section there are 5 reference circuits to show how to design an application circuit with this module.

Reference Circuit configuration 1

- Typical Applications
- Use Normal voltage mode
- Normal voltage mode is entered when the supply voltage is connected to both the VDD and VDDH pins (so that VDD equals VDDH).



Configurations summary for reference circuit 1

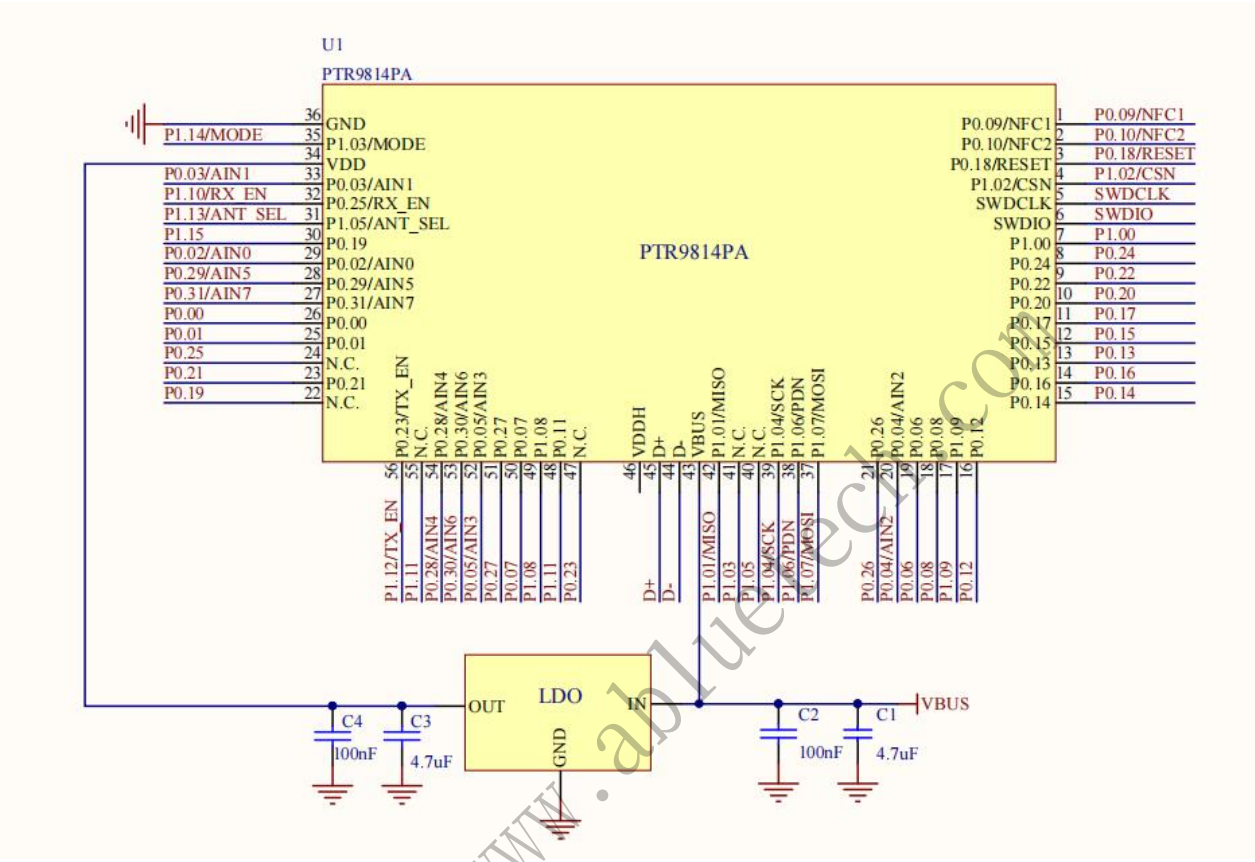
Config no.	Main Supply		EXT Supply Output	USB
	VDDH	VDD		
Config.1	N/A	Battery/Ext.regulator	No	No

Explanation of symbols in reference circuit 1 schematic

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Main supply voltage in normal voltage mode	2.7	3	3.6	V

Reference Circuit configuration 2

- USB Applications
- When using the USB peripheral, 5V USB supply needs to be provided on the VBUS pin.



Configurations summary for reference circuit 2

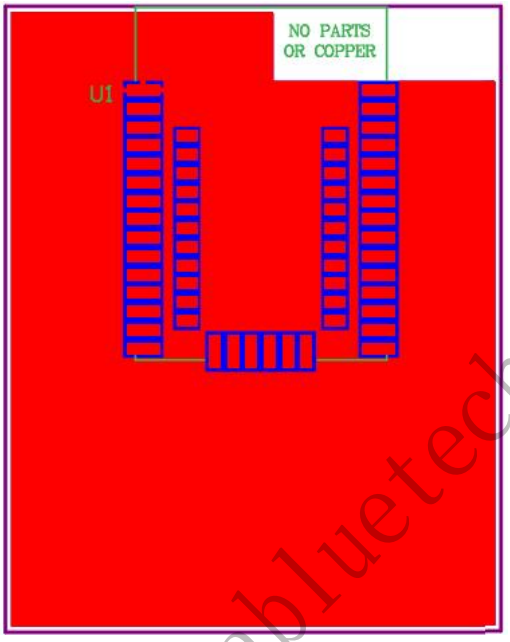
Config no.	Main Supply		EXT Supply Output	USB
	VDDH	VDD		
Config.2	N/A	Battery/Ext.regulator	No	Yes

Explanation of symbols in reference circuit 2 schematic

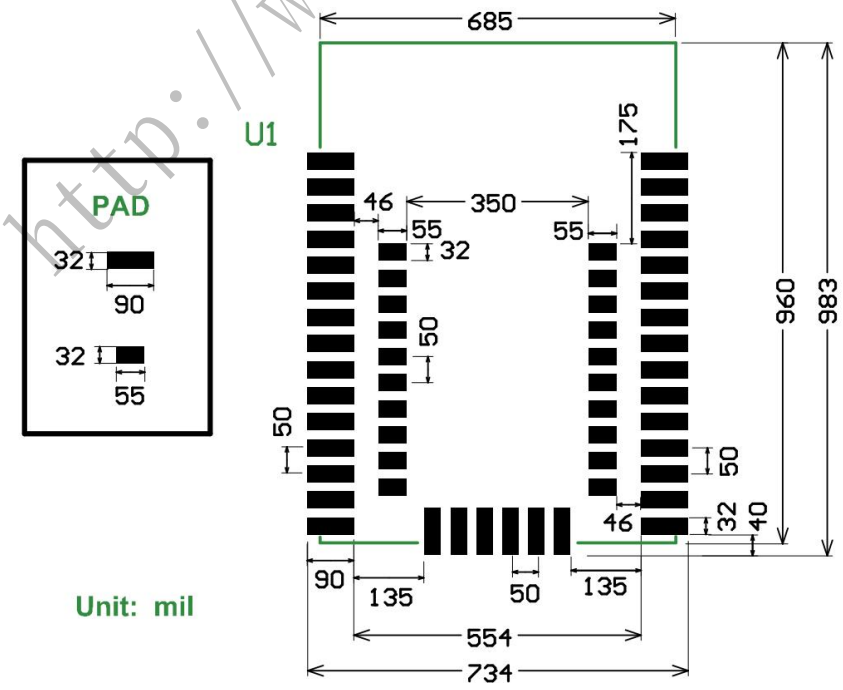
Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Main supply voltage in normal voltage mode	2.7	3	3.6	V
V_{BUS}	Supply voltage on VBUS pin	4.35	5	5.5	V

Recommended RF Layout & Ground Plane:

The module integrated antenna requires a suitable ground plane to radiate effectively. The area under and extending out from the antenna portion of the module should be kept clear of copper and other metal. The module should be placed at the edge of the PCB with the antenna edge facing out. Reducing the ground plane will reduce the effective radiated power. Please add as more as possible via holes on the mother board near the GND pin of module, this will be good for the RF performance of system board.



PCB Footprint （Top View）:



Radio Specifications:

Parameter	Min.	Typ.	Max.	Unit
Frequency Range	2402		2480	MHz
Maximum Output Power		+20		dBm
Rx Sensitivity Level, BLE1 Mbps		-96		dBm
Rx Sensitivity Level, BLE Long Range 125 kbps		-103		dBm
Data Rate on air	125		2000	kbps
Operating Temperature Range	-40	25	85	°C

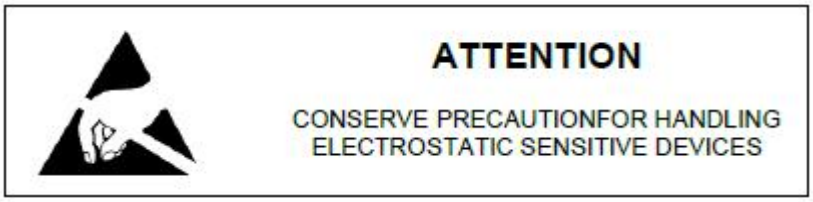
Notes and Cautions:

Design Notes

(1) It is critical to following the recommendations of this document to ensure the module meets the specifications.
(2) Power supply must be free of AC ripple voltage. If such noise is present, it is critical to provide proper filtering and decoupling.
(3) The module should not be stressed mechanically after installation.
(4) Exposing the module to significant temperatures will result in degradation and decreased lifetime.
(5) Keep module away from other high frequency devices which may interfere with operation such as other transmitters and devices generating high frequencies.
(6) Avoid static electricity, ESD and high voltage as these may damage the module.

Handling and Storage

(1) Keep module away from other high frequency devices which may interfere with operation such as other transmitters and devices generating high frequencies.
(2) Do not expose the module to the following conditions: Corrosive gasses such as Cl2, H2S, NH3, SO2, or NOX Extreme humidity or salty air Prolonged exposure to direct Sunlight Temperatures beyond those specified for storage.
(3) Do not apply mechanical stress.
(4) Do not drop or shock the module.
(5) Avoid static electricity, ESD and high voltage as these may damage the module.



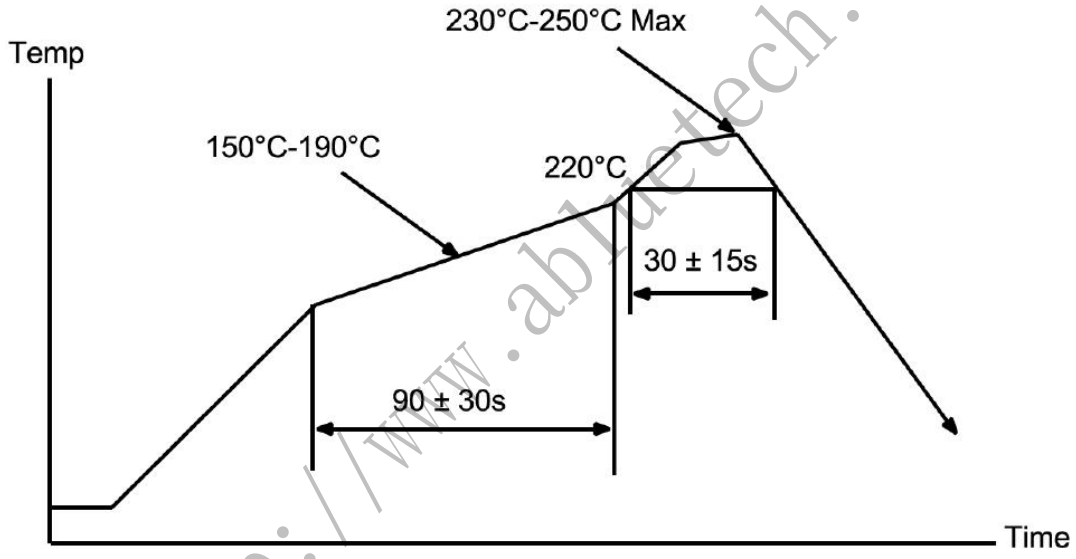
Moisture Sensitivity

All plastic packages absorb moisture. During typical solder reflow operations when SMDs are

mounted onto a PCB, the entire PCB and device population are exposed to a rapid change in ambient temperature. Any absorbed moisture is quickly turned into superheated steam. This sudden change in vapor pressure can cause the package to swell. If the pressure exerted exceeds the flexural strength of the plastic mold compound, then it is possible to crack the package. Even if the package does not crack, interfacial delamination can occur.

Since the device package is sensitive to moisture absorption, it is recommended to bake the product before assembly.

Solder Reflow Temperature-Time Profile



Life Support Applications

Products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Customers using or selling these products for use in such applications do so at their own risk.

Additional Customization

We provide extensive customization, design and manufacturing services to ensure the perfect fit for your product. Our wide selection of modules allows developers to create any number of products. Should you need more information and assistance in integrating this module or developing your product, please contact us.

- Custom Hardware design including Modules, RF and Antenna Design
- Bluetooth Low Energy and Firmware Development
- Mobile Apps for iOS and Android
- Cloud Platform

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Ordering Information:

Part Number	Description
PTR9814PA	Bluetooth 5.3 System on Module, Dual Antenna interface
XANT-IPX-10	2.4GHz FPC Antenna with IPX connector, 2dB gain
XANT-SMA-10	2.4GHz Omni Antenna with SMA connector, 3dB gain
XIPX-SMA-10	IPX to SMA Converter RF cable，use for IPX type connector of RF module to SMA type Antenna.
PTR9814PA-EVB	Evaluation boards for module， with key, LED, I/O extend